Q.P. Code: **16EC3801** **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester (R16) Regular Examinations December 2016

DIGITAL SYSTEM DESIGN

(Common to ES & DECS)

(For Students admitted in 2016 only)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

Q.1	a.	Explain architectural differences between CPLD and FPGA	6M
	b.	Develop an ASM chart of 3-bit synchronous counter with a single control input(EN)	6M
		OR	
Q.2	a.	Design a circuit which generate the no of ones in a given 4-bit number using PLA	8M
	b.	Explain the use of HDL in digital system design..	4M

UNIT-II

Q.3	a.	Discuss about various types of faults in a digital circuits.	8M
	b.	Define fault and Fault diagnosis	4M
		OR	
Q.4	a.	Find out the test vector for detecting SA1 fault at input line x3 and SA0 fault at input line x1 of a given function using path sensitization method F=x1x2+x1x3'x4'+x2x4	6M
	b.	Describe Boolean Difference Method	6M

UNIT-III

Q.5	a.	Describe the steps involved in D-algorithm	8M
	b.	With an example, explain Bridging faults	4M
		OR	
Q.6		With a suitable examples, explain transistion count testing, Random testing and .list out the pros and cons of above methods.	12M

UNIT-IV

Q.7 .Find out the simple coloumn folding by the FCM method and draw the folded PLA.

Coloumn	SSRs
A.	1,2,6
B.	1,5
C.	2,3,5,6
D.	3,4,7,9
E.	2,3,4,8,9
F.	7,8,9
Z1	2,3,4,6,8,9
Z2	1,5,7

12M

OR

Q.8 a. Conduct synchronizing experiment for a given machine and find out shortest synchronizing sequence

PS	NS,Z	
	X=0	X=1
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

6M

b. Define uncertinity Vector ,Trivial uncertinity Vector and succssor tree. 6M

UNIT-V

Q.9 a. Define the races and cycles in asynchronous sequential circuits? 4M

b. Find a circuit that has no static hazards and implement the Boolean function.
$F(A,B,C,D)=\sum(0,2,6,7,8,10,12)$ 8M

OR

Q.10 a. Explain following with an example.
i). Fundamental mode model
ii). State minimization 8M

b. Find out the disapperence faults in a given PLA

	X1	X2	X3	Z1
P1	0	2	1	1
P2	2	1	1	1
P3	1	2	0	1

4M

***** END *****